

# SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

## 3216 PARALLEL BIDIRECTIONAL BUS DRIVER

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL 3216 is a high-speed 4-bit Parallel, Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems

The 3216 driver and receiver gates have three state outputs with PNP inputs. When the drivers or receivers are tri-stated the inputs are disabled, presenting a low current load, typically less than 40  $\mu$ amps, to the system bus structure.

**High Performance—20 ns typical propagation delay**  
**Low Input Load Current—0.25 mA maximum**  
**High Output Drive Capability for Driving System Data Busses**  
**Three-State Outputs**  
**TTL Compatible**  
**16-pin DIP**

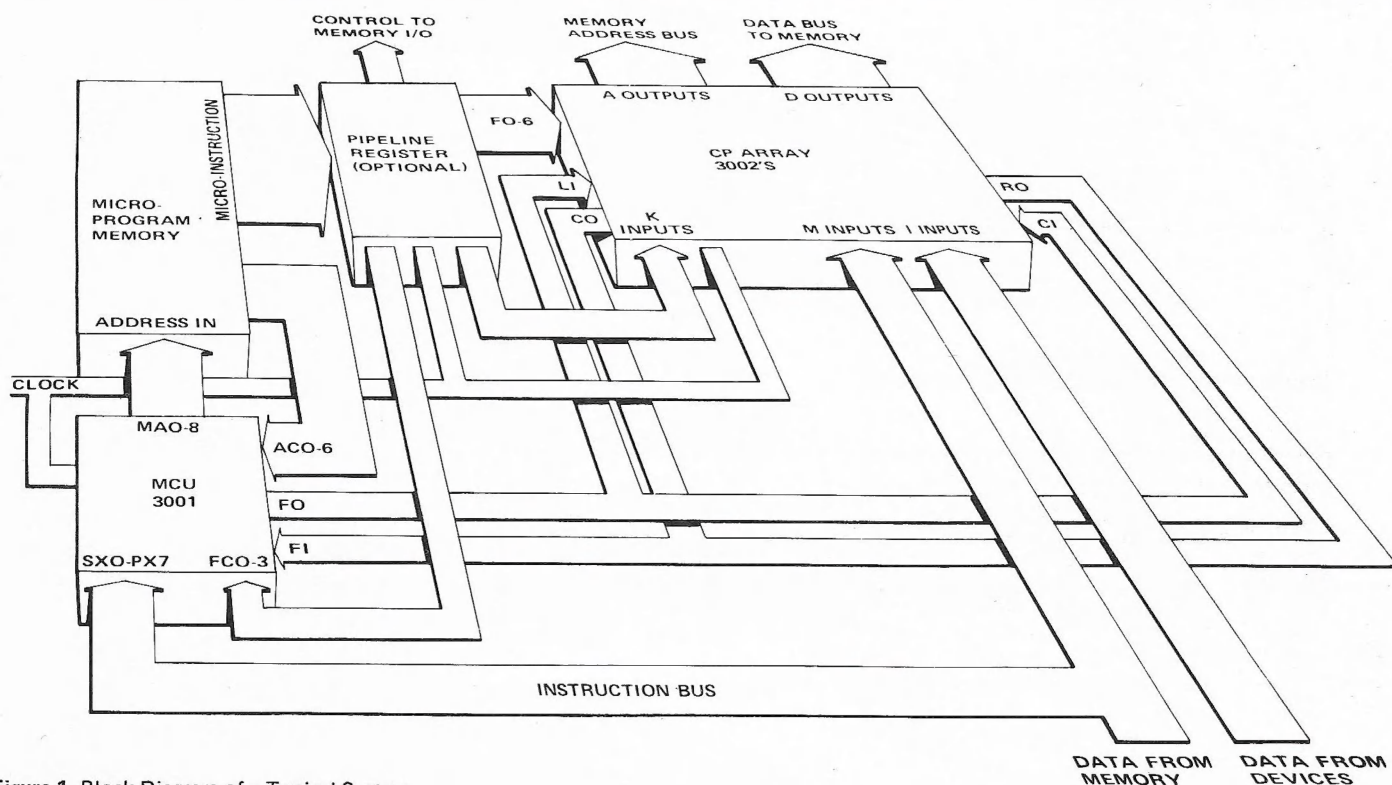


Figure 1. Block Diagram of a Typical System

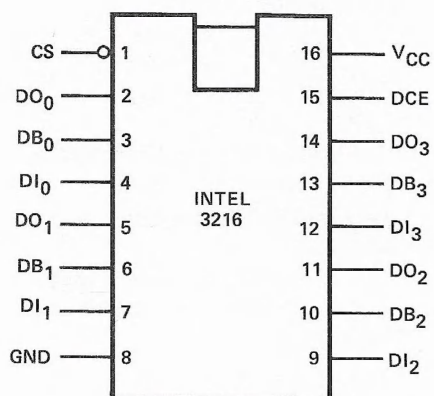
Other members of the INTEL Bipolar Microcomputer Set:

3001 Microprogram Control Unit  
 3002 Central Processing Element  
 3003 Look-Ahead Carry Generator

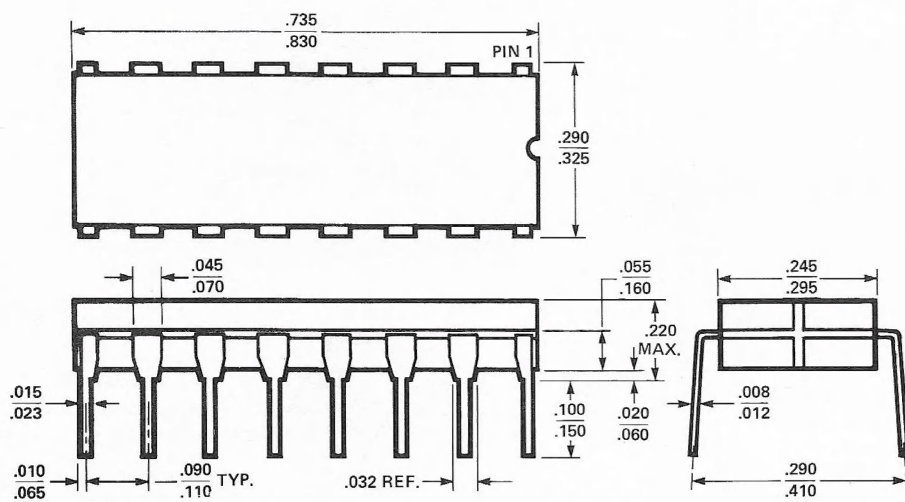
3212 Multi-Mode Latch Buffer  
 3214 Priority Interrupt Control Unit  
 3301A Schottky Bipolar ROM (256 x 4)

3304A Schottky Bipolar ROM (512 x 8)  
 3601 Schottky Bipolar PROM (256 x 4)  
 3604 Schottky Bipolar PROM (512 x 8)

## PACKAGE CONFIGURATION



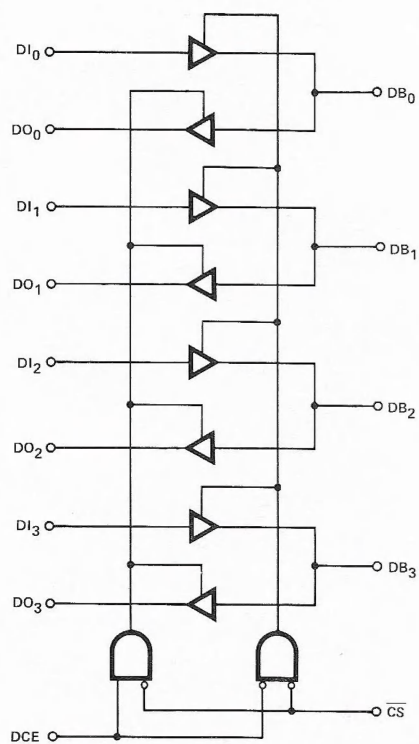
## PACKAGE OUTLINE



## PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1	CS	Chip Select	Active LOW
2,5,11,14	DO	Data Output	
3,6,10,13	DB	Data Bus Bidirectional	
4,7,9,12	DI	Data Input	
8	GND	Ground	
15	DCE	Direction Control Enable	
16	V <sub>CC</sub>	+5 Volt Supply	

## LOGIC DIAGRAM





## D.C. AND OPERATING CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS\*

#### Temperature Under Bias

Ceramic . . . . .	-65°C to +75°C
Plastic . . . . .	0°C to +75°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Currents . . . . . 125 mA

\*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

$T_A = 0^\circ\text{C to } +75^\circ\text{C}$ ,  $V_{CC} = +5V \pm 5\%$

SYMBOL	PARAMETER	LIMITS			UNIT	CONDITIONS
		MIN	TYP	MAX		
$I_{F1}$	Input Load Current DCE, CS		-0.15		mA	$V_F = 0.45$
$I_{F2}$	Input Load Current All Other Inputs		-0.08		mA	$V_F = 0.45$
$I_{R1}$	Input Leakage Current DCE, CS				$\mu\text{A}$	$V_R = 5.25V$
$I_{R2}$	Input Leakage Current DI Inputs				$\mu\text{A}$	$V_R = 5.25V$
$I_{R3}$	Input Leakage Current DB Inputs				$\mu\text{A}$	$V_R = 5.25V$
$V_C$	Input Forward Voltage Clamp				V	$I_C = -5 \text{ mA}$
$V_{IL}$	Input "Low" Voltage				V	
$V_{IH}$	Input "High" Voltage				V	
$I_{CEX}$	Output Leakage				$\mu\text{A}$	$V_O = 0.45V/5.25V$
$I_{CC}$	Power Supply Current		90		mA	
$V_{OL1}$	Output "Low" Voltage		0.3		V	DO Outputs $I_{OL} = 15 \text{ mA}$ Outputs $I_{OL} = 25 \text{ mA}$
$V_{OL2}$	Output "Low Voltage		0.5		V	DB Outputs $I_{OL} = 50 \text{ mA}$
$V_{OH1}$	Output "High" Voltage		4.0		V	DO Outputs $I_{OH} = -1 \text{ mA}$
$V_{OH2}$	Output "High" Voltage		3.0		V	DB Outputs $I_{OH} = -10 \text{ mA}$
$I_{SC}$	Output Short Circuit Current		-35 -75		mA mA	DO Outputs $V_O \cong 0V$ DB Outputs

NOTE: Typical values are for  $T_A = 25^\circ\text{C}$

## A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$

SYMBOL	PARAMETER	LIMITS		UNIT	CONDITIONS
		MIN	TYP <sup>(1)</sup>		
$T_{PD1}$	Input to Output Delay DO Outputs		20	ns	$C_L = 15\text{ pF}$ , $R_1 = 300\Omega$ $R_2 = 600\Omega$
$T_{PD2}$	Input to Output Delay DB Outputs		20	ns	$C_L = 150\text{ pF}$ , $R_1 = 180\Omega$ , $R_2 = 300\Omega$
$T_E$	Output Enable Time		35	ns	DCE
			35	ns	CS
$T_D$	Output Disable Time		25	ns	DCE
			25	ns	CS

NOTE:

(1) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

### TEST CONDITIONS:

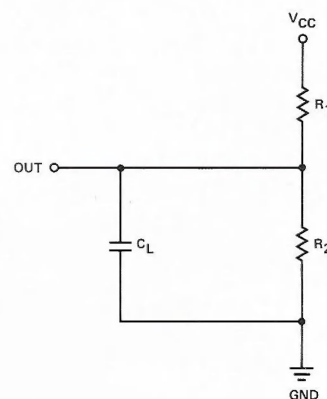
Input pulse amplitude of 2.5V.

Input rise and fall times of 5 ns between 1 and 2 volts.

Output loading is 5 mA and 10 pF.

Speed measurements are made at 1.5 volt levels.

### TEST LOAD CIRCUIT:



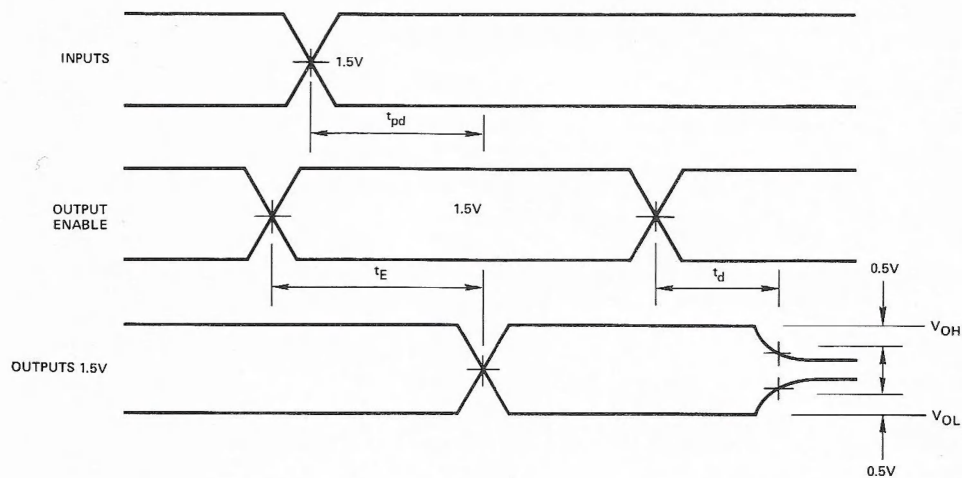
### CAPACITANCE<sup>(2)</sup> $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
$C_{IN}$	Input Capacitance				pF
$C_{OUT}$	Output Capacitance				pF

NOTE:

(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is  $f = 1\text{ MHz}$ ,  $V_{BIAS} = 2.5\text{V}$ ,  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .

# 3216 WAVEFORMS



## ORDERING INFORMATION

**Part Number**   **Description**  
**3216**   4-Bit Parallel,  
 Bidirectional  
 Bus Driver



**Intel Corporation**  
 3065 Bowers Avenue  
 Santa Clara, California 95051  
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 Telex: 34-6372

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1651 East 4th Street  
 Suite 228  
 Santa Ana, California 92701  
 Tel: (714) 835-9642  
 TWX: 910-595-1114

### MID-AMERICA

6350 L.B.J. Freeway  
 Suite 178  
 Dallas, Texas 75240  
 Tel: (214) 661-8829  
 TWX: 910-860-5487

### GREAT LAKES REGION

8312 North Main Street  
 Dayton, Ohio 45415  
 Tel: (513) 890-5350  
 TELEX: 288-004

### EASTERN

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 Lexington, Massachusetts 02173  
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### MID-ATLANTIC

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